

Application No. 09/752,243
Amendment dated: October 17, 2005
Reply to Office Action dated: June 16, 2005

REMARKS/ARGUMENTS

Claims 1-21 are pending and rejected in this application. Claims 1, 2, 9-12, 14, 16, 17, 19, and 20 are rejected under 35 U.S.C. §103(a) as being unpatentable over Smith, et al., US Patent 5,3678,651, in view of Alpha Architecture Handbook ("Alpha"), and Colwell, et al., US Patent 5,524,262. Claims 3-8, 13, 15, 18, and 21 are rejected under 35 U.S.C. §103(a) as being unpatentable over Smith et al., in view of Alpha, Colwell et al., and Rotenburg et al., Trace Cache: A Low Latency Approach to High Bandwidth Instruction Fetching.

Claim Rejections Under 35 U.S.C. §103(a)

Applicant submits that Smith and Alpha provide no motivation to combine, and in fact, teach away from combining. The physical zero register in Alpha is explicitly dedicated as such by the instruction set architecture. "Register R31 is assigned special meaning by the Alpha architecture." (Alpha, 3-1, section 3.1.2 entitled "Integer Registers). As examiner stated in the office action dated August 13, 2004, Smith teaches a "zero-generating apparatus for use with an instruction set architecture without an R0 register." Therefore, Smith and Alpha teach away from combining. Applicant has amended independent claims 1, 14, and 17 to further illustrate this distinction. Colwell and Rotenburg do not cure this deficiency.

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For all the above reasons, the Applicant respectfully submits that this application is in condition for allowance. A Notice of Allowance is earnestly solicited.

The Examiner is invited to contact the undersigned at (408) 975-7500 to discuss any matter concerning this application. The Office is hereby authorized to charge any additional fees or credit any overpayments under 37 C.F.R. §1.16 or §1.17 to Deposit Account No. 11-0600.

Respectfully submitted,
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